Navrachana University

School Of Business And Law

End-Semester Examination November 2017

FYBCA – 1st semester

CA101 : Digital Computer Architecture

Date: 20/11/2017
Time: 10:30am to 12:30pm

Marks: 40
Weightage : 100%

Instructions:

- ➔ Write each answer on a new page
- ➔ Draw neat circuit diagrams wherever required.

Q:1 Give classification of codes with one example each .(5 marks)

Q:2 Implement Boolean function using 4:1 mux $F(A,B,C,D)=\sum m(2,3,5,7,8,9,12)$.(5marks)

Q:3 what is encoder ? Enlist types of encoders also explain priority encoder .(5 marks)

Q:4 Design and explain S-R latch using NAND gates . (5 marks)

OR Design and explain T flipflop (5 marks)

Q:5 Design full subtractor using 1:8 demux

OR Design full adder using 3*8 decoder (4 marks)

Q:6 Prove that 4221 is reflexive system .(2 marks)

Q:7 Perform BCD addition : 245 + 656 .(3 marks)

Q:8 Hamming word received by a receiver is **110111001010**. Assuming even bit parity method verify if received bit sequence is correct or faulty , if faulty identify the bad bit. (5 marks)

OR Reduce the equation in SOP form using K-map for $F(A,B,C,D,E) = \Sigma(0,1,6,7,8,9,10,11,20,21,30,31) + \Sigma d\ (4,5,16,17,26,27)$. Draw circuit for reduced equation.

Q:9 Perform XS-3 addition : 189 – 694 (3marks)

Q:10 Design 3 bit even parity Generator **OR** Design 3 bit odd parity Generator (3 marks)

ALL THE BEST