Enrollment No._____

NAVRACHANA UNIVERSITY
a UGC recognized University

School: School of Engineering and Technology
Program/s: Computer science Engineering
Year: 1st **Semester:** 2nd
Examination: Mid-semester Examination
Examination year: May – 2023

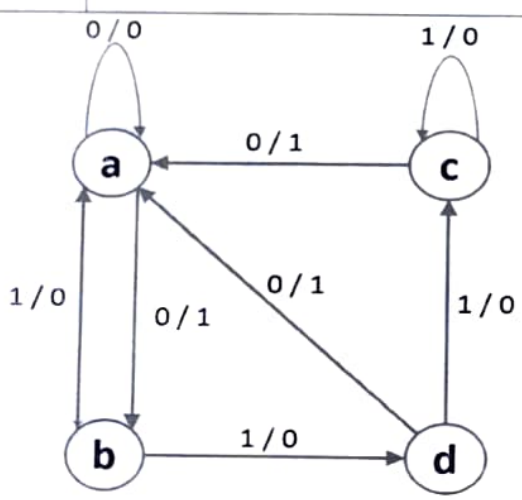
Course Code: CS234 **Course Name:** **Digital logic design**

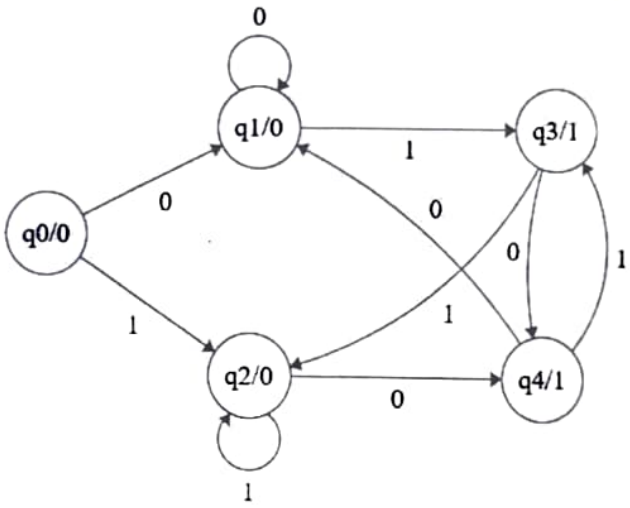
Date: 15/04/2023 **Total Marks:** 40
Time: 2:00 pm to 4:00 pm **Total Pages:** 2

Instructions:
- *Write each answer on a new page.*
- *Use of a calculator is permitted.*
- ** COs=Course Outcome mapping. # BTL=Bloom's Taxonomy Level mapping*

Que. 1	**Attempt any FIVE**	Marks	COs*	BT*
a)	Design the circuit of half and full subtractor with a truth table, k-map and logic diagram.	6	CO3	BT1 BT2 BT4 BT5
b)	Design a 16:1 MUX using 4:1 MUX and explain the working.	6	CO3	BT1 BT3 BT4 BT6
c)	Design a 3 to 8 line decoder with truth table and logic diagram. How a decoder is different from MUX and DEMUX?	6	CO3	BT2 BT3 BT5 BT6
d)	Design a Binary to grey code converter with a truth table, K-map and logic circuit.	6	CO3	BT1 BT2 BT4 BT5
e)	Write a short note on the following: (i) Weighted and non-weighted code (ii) 2-bit magnitude comparator	6	CO2	BT1 BT2 BT4 BT5
f)	(i) Perform the following decimal subtraction in BCD by 9's complement. 305.5-168.8 (ii) Perform the addition in the XS-3 code: 247+359	6	CO2	BT1 BT3 BT4 BT6

Que.2	Attempt any TWO			
a)	Define and explain the terms 'state table' and 'state diagram'. Compare and contrast Moore Model and Mealy Model.	5	CO2	BT1 BT2 BT3
b)	Draw the circuit diagram and discuss the state table for either SR flip flop or JK flip flop.	5	CO2, CO3	BT3 BT4
c)	Derive the state tables from following given state diagrams.	5	CO3	BT4 BT5 BT6





**********End of Question Paper**********